REMARKS

Applicants amend claims 1-3, 5, 7-13 and cancel claim 4. Further, Applicants add new claims 14-18. No new matter is added by way of the amended and newly added claims, for which Applicants respectfully request entry. The clarifying amendments and newly added claims are fully supported by the specification.

Objection to the Specification under 35 U.S.C. § 132

Applicants submitted a substitute specification with the Office Action reply mailed on November 17, 2003, addressing the correction of any errors and other information related to the pending U.S. patent application. The substitute specification includes no new matter. Specifically, Applicants respectfully direct the Office to the originally filed drawings, filed on August 18, 2000. Figure 6a illustrates "Data Organization: Singly Linked List" and Figure 6b illustrates "Data Organization: Byte Stream." The Figures were amended to comply with formal drawing requirements in order to file formal drawings on November 17, 2003. Consequently, the illustrated text of the Figures were moved into the appropriate sections of the substitute specification. Thus, Applicants respectfully submit that no new matter has been added to the substitute specification.

Claim Rejections Under 35 U.S.C. § 101

The Examiner rejected claims 7-10 under 35 U.S.C. § 101. Applicants amend independent claim 7, as suggested by the Examiner in paper number 8. Accordingly, Applicants respectfully request the withdrawal of the rejection under 35 U.S.C. § 101.

Claim Rejection Under 35 U.S.C. § 112

Further, the Examiner rejected claim 10 under 35 U.S.C. § 112, first paragraph and second paragraphs. As amended, claim 10 is fully supported by the substitute specification previously amended to include illustrated text from Figures 6a and 6b, which were originally filed on August 18, 2000. Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. § 112 rejection.

Claim Rejections Under 35 U.S.C. § 102(b)

The Examiner rejected claims 1-2, 5, 7-8, and 10-11 under 35 U.S.C. § 102(b) as being anticipated by Sollars (U.S. Patent No. 5,900,025). Applicants respectfully traverse.

Sollars discloses a processor having a hierarchical control register file. Further, the hierarchical control register files are coupled to execution units and caches. However, the clarifying amendments to independent claims 1, 5, 7, and 12 recite a register file coupled to an execution unit. A bypass circuit is coupled to the register file and the execution unit and further, a backing register file is coupled to the register file such that an instruction has registering windowing capability or has the capability to use the backing register file in native mode, wherein the native mode is the capability to address each register of the backing register file by way of addresses or at random.

The reference does not disclose the coupling of the register file, the execution unit, the bypass circuit, and the backing register file that is responsively coupled to an instruction having multiple capabilities. As such, the reference does not anticipate the claimed invention. Accordingly, Applicants respectfully request the withdrawal of the 35 U.S.C. § 102(b) rejection and allowance of claims 1-2, 5, 7-8, and 10-11.

Claim Rejections Under 35 U.S.C. § 103(a)

The Office offers Sollars' hierarchical control register files in combination with Wilhelm et al.'s (U.S. Patent No. 5,956,747) memory hierarchy 24 to reject claims 3-4, 9, and 12-13 under 35 U.S.C. § 103(a). Applicants respectfully traverse.

Sollars discloses multiple control register levels, classified as a system level, a context level, and a thread level. The system level controls overall system operation while the context level controls concurrent execution of processes in multiple contexts. The thread level controls concurrent execution of multiple peer process threads of the concurrently executing threads of the concurrently executing contexts. Further, a fourth level includes partitioned subsets of the auxiliary control register file 20b to control executions of macro-tap library routines. By using the multiple control register levels, Sollars discloses a method to control a computer system in an organized manner. Thus, the reference discloses that each control register file is used for a different purpose by the classification system. To one of ordinary skill in the art, the classification system means that different types of instructions are directed to different register files. Further, Sollars does not disclose that a control register level is operationally coupled to an instruction with multiple capabilities.

However, the claimed invention recites a register file coupled to an execution unit, such that the register file is further coupled to a backing register file capable of receiving instruction with multiple capabilities. Specifically, the backing register file is operationally

and responsively coupled to an instruction, such that the instruction has registering windowing capability or has the capability to use the backing register file in native mode. Native mode is the capability to address each register of the backing register file by way of addresses or at random. As compared to the claimed invention, the reference does not disclose that instructions operatively coupled to a backing register file are capable of having multiple capabilities. On the contrary, Sollars discloses using each control register to execute one type of instruction to control the computer system in an organized manner. Thus, Sollars teaches away from a backing register file operatively coupled to an instruction having multiple capabilities.

When Sollars is combined with Wilhelm et al., which only discloses a memory hierarchy 24, there is no reference to an instruction with multiple capabilities being operationally and responsively coupled to a backing register file. Specifically, the combination discloses multiple control register files such that one register file can be coupled to a main memory. However, there is no teaching or suggestion of an instruction with multiple capabilities operatively coupled to a backing register file, which is in turn coupled to a register file. Thus, Applicants respectfully request the withdrawal of the 35 U.S.C § 103(a) rejection and allowance of claims 3-4, 9, and 12-13.

Applicants respectfully request a Notice of Allowance based on the foregoing remarks. If the Examiner has any questions concerning the present amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6900. If any other fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. SUNMP298). A copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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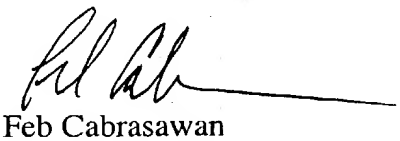

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